Abstract

The urgency of a new framework in wireless digital transmission which should allow for higher bit rate, lower latency and tighter delay constraints, led us to investigate the fundamental building blocks which, at the circuital/device level, will foster a change towards more efficient communication schemes, delivering a more satisfactory end user experience. Specifically, this work deals with the inherently analog devices, found at the core of each transceiver module and capable of providing the carrier signal; these are the oscillators. In particular, two distinct classes of oscillators are regarded central to our contribution. One class is constituted by N-push oscillators, which thanks to coupling effect of N identical core oscillators allow N-fold harmonic generation (and thus high frequency transmission). The second class is constituted by wideband tunable oscillators, whose topology derives from a feedback distributed amplifier and therefore called distributed oscillators. The introductory part of this work, deals with their operation principles in great detail. Moreover, nonlinear numerical microwave circuit simulation techniques have been thoroughly reviewed. A triple-push oscillator topology has been initially considered. Provided a certain phase distribution is maintained among the oscillating elements, the output power of the third harmonic increases while the lower order harmonics cancel out, which represents the default operating mode. A design strategy relying on the Harmonic Balance parametric analysis of the oscillating voltage at a selected node in the coupling network with respect to coupling phase and coupling strength is presented, to the aim of quenching undesired oscillation modes. Moreover the design of a four stage reverse mode distributed voltage controlled oscillator (DVCO) has been described. All the design steps have been reported, from a very idealized, purely behavioral design to a very concrete one, involving details derived from electromagnetic simulations. Harmonic Balance techniques were used to evaluate its tuning function, output power and DC current consumption, which have been completely characterized across the tuning bandwidth. Finally, a method for an optimized design with reduced variations in the output power has been presented. An alternative implementation, targeting wider tuning ranges/ higher oscillation frequencies was introduced. The measurements performed on the fabricated prototypes revealed good agreement with the simulation results, confirming the validity of the approach.